A1

emulation. Moreover, the invention is not limited to the exact implementation details of the exemplary embodiment used herein for illustrative purposes.

Please replace the paragraph beginning at page 10, line 21 with the following:

Referring now to FIGURE 2, an architecture for implementation of an embodiment of an ICE system of the present invention is illustrated as system 200. In system 200, a host computer 210 (e.g., a personal computer based on a PENTIUM® class microprocessor) is interconnected (e.g., using a standard PC interface 214 such as a parallel printer port connection, a universal serial port (USB) connection, etc.) with a base station 218. The host computer 210 generally operates to run an ICE computer program to control the emulation process and further operates in the capacity of a logic analyzer to permit a user to view information provided from the base station 218 for use in analyzing and debugging a device under test or development. According to an embodiment of the present invention microcontroller 232, mounted on a pod, comprises file register 236, SRAM 237, CPU 238, memory 240, and a program counter 239.

A2

Please replace the paragraph beginning at page 11, line 22 with the following:

The FPGA of the base station 218 of the current embodiment is designed to emulate the core processor functionality (microprocessor functions, Arithmetic Logic Unit functions, RAM, and ROM memory functions) of the Cypress MicroSystems CY8C25xxx/26xxx series microcontrollers. The CY8C25xxx/26xxx series of microcontrollers also incorporate limited I/O functions and an interrupt controller as well as programmable digital and analog circuitry. This circuitry need not be modeled using the FPGA 220. Instead the I/O read information, interrupt vector and other information can be passed to the FPGA 220 from the microprocessor 232 via interface 227 as will be described later.

A3

Please replace the paragraph beginning at page 12, line 19 with the following:

In the designing of a microcontroller or other complex circuit such as the microcontroller 232, it is common to implement the design using the VERILOG® language (or other suitable language). Thus, it is common that the full functional design description of the microcontroller is fully available in a software format. The base station 218 of the current embodiment is based upon the commercially available SPARTAN® series of FPGAs from Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124. The VERILOG® description can be used as the input to the FPGA design and synthesis tool available from the FPGA manufacturer to realize the virtual microcontroller 220 (generally after timing adjustments and other debugging). Thus, design and realization of the FPGA implementation of an emulator for the microcontroller (virtual microcontroller) or other device can be readily achieved by use of a VERILOG description along with circuitry to provide interfacing to the base station and the device under test (DUT).

VERSION OF AMENDMENTS WITH CHANGES SHOWN:

IN THE SPECIFICATION

Please replace the paragraph beginning at page 10, line 9 with the following:

A commercial ICE system utilizing the present invention is available from Cypress [Micro Systems,] MicroSystems, Inc., for the CY8C25xxx/26xxx series of microcontrollers. Detailed information regarding this commercial product is available from Cypress [Micro Systems, inc.,] MicroSystems, Inc., 22027 17th Avenue SE, Suite 201, Bothell, WA 98021, [Bothel, WA] in the form of version 1.11 of ["PsoC Designer:] "PSOC DESIGNER: Integrated Development Environment User Guide", which is hereby incorporated by reference. While the present invention is described in terms of an ICE system for the above exemplary microcontroller device, the invention is equally applicable to other complex circuitry including microprocessor and other circuitry that is

suitable for analysis and debugging using in-circuit emulation. Moreover, the invention is not limited to the exact implementation details of the exemplary embodiment used herein for illustrative purposes.

Please replace the paragraph beginning at page 10, line 21 with the following:

Referring now to FIGURE 2, an architecture for implementation of an embodiment of an ICE system of the present invention is illustrated as system 200. In system 200, a host computer 210 (e.g., a personal computer based on a [Pentium™] PENTIUM® class microprocessor) is interconnected (e.g., using a standard PC interface 214 such as a parallel printer port connection, a universal serial port (USB) connection, etc.) with a base station 218. The host computer 210 generally operates to run an ICE computer program to control the emulation process and further operates in the capacity of a logic analyzer to permit a user to view information provided from the base station 218 for use in analyzing and debugging a device under test or development. According to an embodiment of the present invention microcontroller 232, mounted on a pod, comprises [of] file register 236, SRAM 237, CPU 238, memory 240, and a program counter 239.

Please replace the paragraph beginning at page 11, line 22 with the following:

The FPGA of the base station 218 of the current embodiment is designed to emulate the core processor functionality (microprocessor functions, Arithmetic Logic Unit functions, RAM, and ROM memory functions) of the Cypress MicroSystems CY8C25xxx/26xxx series microcontrollers. The CY8C25xxx/26xxx series of [microcontroller] microcontrollers also incorporate limited I/O functions and an interrupt controller as well as programmable digital and analog circuitry. This circuitry need not be modeled using the FPGA 220. Instead the I/O read information, interrupt vector and other information can be passed to the FPGA 220 from the microprocessor [232via] 232 via interface 227 as will be described later.

Please replace the paragraph beginning at page 12, line 19 with the following:

In the designing of a microcontroller or other complex circuit such as the microcontroller 232, it is common to implement the design using the [Verilog ™] VERILOG® language (or other suitable language). Thus, it is common that the full functional design description of the microcontroller is fully available in a software format. The base station 218 of the current embodiment is based upon the commercially available [Spartan ™] SPARTAN® series of FPGAs from Xilinx, [inc.,] Inc., 2100 Logic Drive, San Jose, CA 95124. The [Verilog ™] VERILOG® description can be used as the input to the FPGA design and synthesis tool available from the FPGA manufacturer to realize the virtual microcontroller 220 (generally after timing adjustments and other debugging). Thus, design and realization of the FPGA implementation of an emulator for the microcontroller (virtual microcontroller) or other device can be readily achieved by use of [Verilog] a VERILOG description along with circuitry to provide interfacing to the base station and the device under test (DUT).

SUPPORT FOR AMENDMENTS

Support for the amendments herein can be found throughout the specification as originally filed. The present amendment intends to clarify references to trademarks of Cypress MicroSystems, Inc. and others (see, e.g., M.P.E.P. § 608.01(v) and the attached printouts from http://tess.uspto.gov/, notably the "PENTIUM," "VERILOG" and "SPARTAN" trademark registration information therein, and http://www.cypressmicro.com/corporate/CY_Announces_nov_13_2000.html). No new matter is introduced.